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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/978,530	10/16/2001	Ronald E. Garcis	30GF (9131)	4988
26127	7590	11/03/2004	EXAMINER	
DYKEMA GOSSETT PLLC 39577 WOODWARD AVENUE SUITE 300 BLOOMFIELD HILLS, MI 48304-5086			SURYAWANSHI, SURESH	
			ART UNIT	PAPER NUMBER
			2115	

DATE MAILED: 11/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/978,530	Applicant(s) GAREIS ET AL.	
	Examiner Suresh K Suryawanshi	Art Unit 2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 October 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-27 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-27 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 16 October 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>10/16/01</u> | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 1-27 are presented for examination.

Drawings

2. The drawings are objected to because Fig. 4 contains multiple figures. Fig. 4 should be labeled as Fig. 4a, Fig. 4b, Fig. 4c, Fig. 4d, Fig. 4e, Fig. 4f and Fig. 4g. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States;

4. Claims 1-3 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Cieri et al (US Patent no 5,093,804¹).

5. As per claim 1, Cieri et al teach

generating in the controlling element a control signal in the form of sequential pulse frames, each frame having at least one control pulse defining said control information [col. 20, lines 10-13];

transmitting said control signal to said controlled element and generating in the controlled element a clock pulse for each control pulse such that said clock pulse follows said control pulse by a pre-selected time interval on each frame, there being one clock pulse for each control pulse such that there is a fixed time relationship between each control pulse and each clock pulse [col. 20, lines 14-21];

¹ Cieri et al is a prior art reference cited by applicants in IDS dated 10/16/01.

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generating in the controlled element a diagnostic signal independent of the control signal but which is indicative of operating parameters of the controlled element [col. 20, lines 22-25];
and

using said clock pulse on each frame to cause a sampling of said control information and to cause a transmission of a value of said diagnostic signal to said controlling element [col. 20, lines 26-29];

wherein the I/O circuit comprises a switch processor, a plurality of signal conditioning circuits, and a switch section [Fig. 4; col. 7, line 65 – col. 8, line 21; an equivalent definition of a switch processor as described by applicants at page 14, para [0055]; col. 10, lines 59-66].

6. As per claim 2, Cieri et al teach that each frame of the control signal further includes a no-pulse time interval during which no pulses appear defining the end of a frame [col. 20, lines 30-33].

7. As per claim 3, Cieri et al teach that each frame of said control signal includes a series of pulses defining said control information [col. 20, lines 34-36].

8. As per claim 9, Cieri et al teach that series of pulses is pulse width modulated [col. 20, lines 37-38].

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

10. Claims 10-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cieri et al (US Patent no 5,093,804) in view of Fordham et al (US Patent no 5,136,528).

11. As per claim 10, Cieri et al teach that diagnostic signal comprises a multi-bit digital signal and the number of bits transmitted to said controlling element on each frame equals the number of pulses in said series of pulses in the same frame [col. 20, lines 39-43].

Cieri et al do not expressly disclose about the multi-bit digital signal is determined by firmware loaded on the switch processor. But, Cieri et al clearly disclose about the switch processor as detailed in claim 1 and there is a coding means to help the switch processor to perform its job [col. 21, lines 36-42]. However, Fordham et al clearly disclose that it is well know in the art to have a firmware with a switch processor [col. 12, lines 39-40]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as both teach about a switch module. Moreover, a routineer will modify the switch processor of Cieri et al with the switch processor having a firmware as disclosed by Fordham et al to enhance the performance of the system and make it more flexible.

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12. As per claim 11, Cieri et al disclose an input/output (I/O) circuit comprising a switch processor, a plurality of signal conditional circuits, and a switch [Fig. 3, 4, col. 7, line 65 – col. 8, line 21; an equivalent definition of a switch processor as described by applicants at page 14, para [0055]; col. 10, lines 59-66].

Cieri et al do not expressly disclose that the switch processor comprises firmware program. But, Cieri et al clearly disclose about the switch processor as detailed above and there is a coding means to help the switch processor to perform its job [col. 21, lines 36-42]. However, Fordham et al clearly disclose that it is well known in the art to have a firmware with a switch processor [col. 12, lines 39-40]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as both teach about a switch module. Moreover, a routineer will modify the switch processor of Cieri et al with the switch processor having a firmware as disclosed by Fordham et al to enhance the performance of the system and make it more flexible.

13. As per claim 12, Cieri et al disclose the invention substantially. Cieri et al do not expressly disclose about the series of pulses comprising two to six pulses. But, Cieri et al clearly disclose that the series of pulses can contain either two or four [col. 8, lines 25-27]. However, a routineer in the art would know to increase or decrease the number of pulses as needed. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the series of pulses to contain two to six pulses instead of two to four. Moreover, having extra pulses will allow one to provide some extra information as needed.

14. As per claim 13, Cieri et al disclose that the switch processor comprises a zero crossing turn-on and turn-off feature [Fig. 8; col. 13, lines 61-64].

15. As per claim 14, Cieri et al disclose the invention substantially. Cieri et al do not expressly disclose about an analog-to-digital converter circuit for converting signals. But, a routineer would know about it as it is well know circuitry in the art. However, Fordham et al clearly disclose about an analog-to-digital circuitry [col. 15, lines 3-12; col. 16, lines 30-36]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as both teach about a switch module.

16. As per claim 15, Cieri et al teach that the switch processor receives a signal representative of the switch section current [Fig. 4; col. 11, lines 18-33].

17. As per claim 16, Cieri et al teach that the switch processor causes the switch to be turned off immediately upon detection of a first threshold current level [Fig. 4; ON/OFF; col. 11, lines 18-33].

18. As per claim 17, Cieri et al teach that the switch processor causes the switch to be turned off after a predetermined period of time [col. 14, line 51 – col. 15, line 19; Fig. 4].

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19. As per claim 18, Cieri et al teach that the switch processor reports an overcurrent diagnostic signal, but does not turn off the switch, upon detection of a switch current level of a third threshold level, the third threshold level being lower than the second threshold level [Fig. 10].

20. As per claim 19, Cieri et al teach that the switch processor generates diagnostic codes for one or more of: over temperature conditions, short circuit conditions, over current conditions, low voltage conditions, and high voltage conditions based on input signals from the conditioning circuits [Fig. 10].

21. As per claim 20, Cieri et teach

an operations control including a switch processor for providing a control signal in the form of sequential pulse frames, each frame having at least one control pulse defining a desired control status [col. 20, lines 46-49; Fig. 4; col. 7, line 65 – col. 8, line 21; an equivalent definition of a switch processor as described by applicants at page 14, para [0055]]; and

at least one I/O point connected to the operations control unit and having an output control device subject to activation and deactivation as an operative condition in accordance with said control status and further including: (1) timing means responsive to each control pulse to generate a clock pulse which follows said control pulse by a pre-selected time interval on each

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frame, there being one clock pulse for each control pulse such that there is a fixed time relationship between such pulses; (2) means connected to the I/O point for providing a diagnostic signal having a value indicative of the operative condition of the I/O point; (3) means connected to receive each clock pulse and responsive to each clock pulse on each frame to cause a sampling of each control pulse to determine the desired control status; and (4) means connected to receive each clock pulse and the diagnostic signal and responsive to said clock pulse on each frame to cause a transmission of a value of said diagnostic signal to the operations control unit [col. 20, line 50 – col. 21, line 2].

Cieri et al do not expressly disclose about a firmware loaded on the switch processor. But, Cieri et al clearly disclose about the switch processor as detailed in above and there is a coding means to help the switch processor to perform its job [col. 21, lines 36-42]. However, Fordham et al clearly disclose that it is well known in the art to have a firmware with a switch processor [col. 12, lines 39-40]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as both teach about a switch module. Moreover, a routineer will modify the switch processor of Cieri et al with the switch processor having a firmware as disclosed by Fordham et al to enhance the performance of the system and make it more flexible.

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22. As per claim 21, Cieri et al teach that operations control unit provides said control signal such that each frame includes a series of pulses followed by a no-pulse time interval during which no pulses occur, said no-pulse time interval defining the end of a frame [col. 21, lines 3-7].

23. As per claim 22, Cieri et al teach that at least the first two pulses of each frame are pulse width modulated redundantly to determine the control status [col. 21, lines 8-10].

24. As per claim 23, Cieri et al teach

output control means responsive to be activated and deactivated by a command signal [col. 21, lines 16-17];

an operations controller generating at least one control signal in the form of sequential pulse frames, each frame of which contains at least one pulse defining a control status for the output control means and a time interval without pulses defining the end of the frame whenever said interval reaches a first pre-selected time duration [col. 21, lines 18-24];

a communications and control section receiving said control signal and including means responsive to said at least one pulse to provide said command signal for activating and deactivating said output control means in accordance with said control status for each frame and

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means responsive to said time interval for synchronizing operation of said communications and control section with each frame; sensing means providing status signals indicative of the operative condition of said output control means [col. 21, lines 25-35]; and

wherein said communications and control section includes a switch processor with coding means for receiving said status signals and responsive thereto to produce a diagnostic signal which is updated on each frame of said control signal and first selector means for transmitting said diagnostic signal to said operations controller on each frame of said control signal [col. 21, lines 36-42; Fig. 4; col. 7, line 65 – col. 8, line 21; an equivalent definition of a switch processor as described by applicants at page 14, para [0055]].

Cieri et al do not expressly disclose about a firmware loaded on the switch processor. But, Cieri et al clearly disclose about the switch processor as detailed in above and there is a coding means to help the switch processor to perform its job [col. 21, lines 36-42]. However, Fordham et al clearly disclose that it is well known in the art to have a firmware with a switch processor [col. 12, lines 39-40]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as both teach about a switch module. Moreover, a routineer will modify the switch processor of Cieri et al with the switch processor having a firmware as disclosed by Fordham et al to enhance the performance of the system and make it more flexible.

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25. As per claim 24, Cieri et al teach that each frame of said control signal contains a series of pulses defining said control status [col. 21, lines 43-45].

26. As per claim 25, Cieri et al teach that at least the first two pulses of each frame are pulse width modulated redundantly to determine the command signal for activating and deactivating the output control means [col. 21, line 46 – col. 22, line 2].

27. As per claim 26, Cieri et al teach that communications and control section further includes second selector means responsive to said time interval to cause said output control means to assume a pre-selected state whenever the time duration of said interval reaches a second pre-selected value [col. 22, lines 3-8].

28. As per claim 27, Cieri et al teach that a plurality of output control means and a corresponding plurality of communications and control sections, and wherein said operations controller generates a plurality of control signals providing one control signal for each communications and control section [col. 22, lines 9-14].

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29. Claims 4-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cieri et al (US Patent no 5,093,804).

30. As per claims 4-8, Cieri et al disclose the invention substantially. Cieri et al do not expressly disclose about the series of pulses comprising two to six pulses. But, Cieri et al clearly disclose that the series of pulses can contain either two or four pulses [col. 8, lines 25-27]. However, a routineer in the art would know to increase or decrease the number of pulses as needed. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the series of pulses to contain two to six pulses instead of two to four. Moreover, having extra pulses will allow one to provide some extra information as needed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suresh K Suryawanshi whose telephone number is 571-272-3668. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sks

October 25, 2004

Dennis M. Butler

Dennis M. Butler
Primary Examiner